

APPARATUS AND METHOD TO REDUCE MEMORY FOOTPRINTS IN PROCESSOR ARCHITECTURES

ABSTRACT

The present invention provides an apparatus and method to reduce the memory footprint of a processor architecture by structuring processor code to be stored in an external device, and transferring into the processor certain code and associated data as it is needed. The processor code or algorithm is divided into a controlling piece and a working piece. The controlling piece can be located on a low-MIPS, high memory-footprint device, whereas the working piece can be located on a high-MIPS, low memory-footprint device. The working piece can also be broken down into phases or segments, which are put in a data store. The segments are then transferred, on an as-needed basis along with associated data, from the store into the constrained memory of the low memory-footprint device. Transfer is facilitated by a segment manager which can be processed from the low-MIPS device, or alternatively from the high-MIPS device.

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